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09/387,857	09/01/1999	FUMITAKA SUGAYA	1776/00039	3099

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EXAMINER
NOVACEK, CHRISTY L

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

. Office Action Summary	Application No. 09/387,857	Applicant(s) SUGAYA, FUMITAKA
	Examiner Christy L. Novacek	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-36 and 38-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-31* is/are allowed.

6)☒ Claim(s) *32-36 and 38-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/059,590* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to the amendment filed December 27, 2001.

Response to Amendment

The amendment to the specification is sufficient to overcome the objections to the title and the objection to page 1, lines 14-15 of page 7 and lines 23-25 of page 8 of the specification as stated in the previous Office Action. Therefore, these objections are withdrawn. However, the amendment failed to overcome the objection to page 8, lines 7-8 and failed to address the objection to page 9, lines 15-17 and pg. 10, lines 10-11 of the specification. Therefore, these rejections are maintained and repeated below for clarity.

The amendment of claim 32 is sufficient to overcome the objection to claim 32 as stated in the previous Office Action. Therefore, this rejection is withdrawn.

The amendment of claims 28, 32 and 36 are sufficient to overcome the rejection of claims 28-45 under 35 U.S.C. 112, second paragraph that was stated in the previous Office Action. Therefore, this rejection is withdrawn.

The limitations added to claim 32 are sufficient to overcome the Schoenfeld reference. Therefore, the rejections of claims 32-34 under 35 U.S.C. 102(e) as being anticipated by Schoenfeld and claim 35 under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld are hereby withdrawn.

The limitations added to claim 36 are sufficient to overcome the Tseng reference. Therefore, the rejections of claims 36-38 and 40 under 35 U.S.C. 102(e) as being anticipated by Tseng are hereby withdrawn.

The limitations added to claim 36 are sufficient to overcome the Iwamatsu reference. Therefore, the rejections of claims 36-39 and 41 under 35 U.S.C. 102(b) as being anticipated by Iwamatsu are hereby withdrawn.

Drawings

The drawings are objected to because in Fig. 1A reference element "1" points to the same object as "2". In Fig. 10A, reference element "31" points to the same object as "32". Correction is required. This objection was made in the previous Office Action mailed September 11, 2001. Applicant's response filed on December 27, 2001 states "Withdrawal of the objection to Figs. 1A and 10A is requested in light of the drawing correction enclosed herein." However, the response filed does not have any drawing corrections attached thereto. A proposed drawing correction or corrected drawings are required in reply to this Office Action to avoid **abandonment** of the application. The objection to the drawings will **not** be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Lines 13-14 of claim 32, as amended, recite the limitation of etching the first conductive layer until a first opening in the first conductive film extends to the element isolation structure. The specification provides support only for etching a gate electrode using a mask such that an element isolation structure is exposed (Fig. 1C, 4B, 6B and 8D). Lines 4-10 of claim 32 clearly distinguish the first conductive layer from the gate electrode. The specification does not provide

support for etching a conductive layer other than the gate electrode such that the element isolation structure is exposed.

Claim 43 recites the limitation of "the ninth step of forming an insulating interlayer on an entire surface of the substrate". However, claim 42, upon which claim 43 depends recites etching the first conductive film until an "insulating interlayer" is exposed in the sixth step. The specification does not provide support for forming another insulating interlayer after the first insulating interlayer is deposited.

The disclosure is objected to because of the following informalities:

The phrase "opposing the second conductive film to the first conductive film through the dielectric film" is not understood by the Examiner. This phrase occurs on pg. 8, lines 7-8 and 23-25, pg. 9, lines 15-17, pg. 10, lines 10-11 of the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 32-35 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Lines 13-14 of claim 32, as amended, recite the limitation of etching the first conductive layer until a first opening in the first conductive film extends to the element isolation structure. The specification provides support only for etching a

gate electrode using a mask such that an element isolation structure is exposed (Fig. 1C, 4B, 6B and 8D). Lines 4-10 of claim 32 clearly distinguish the first conductive layer from the gate electrode. The specification does not provide support for etching a conductive layer other than the gate electrode such that the element isolation structure is exposed.

Claim 43 recites the limitation of "the ninth step of forming an insulating interlayer on an entire surface of the substrate". However, claim 42, upon which claim 43 depends recites etching the first conductive film until an "insulating interlayer" is exposed in the sixth step. The specification does not provide support for forming another insulating interlayer after the first insulating interlayer is deposited.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 42-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 42 recites the limitation "said insulating interlayer" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 36 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Schoenfeld et al. (US 6,010,932, previously cited).

In reference to claim 36, Schoenfeld discloses a first conductive film (128) is formed in an insulating film region (126) on a semiconductor substrate (102) (Fig. 1). A mask pattern (130) having two openings (140/142) of different dimensions is formed on the first conductive film and the mask is used to divide the first conductive film while it is conformed to a shape of one of the openings (142) and at least one recess is simultaneously formed while the surface of the first conductive film is conformed to the shape of the other opening (Fig. 2-3; col. 4, ln. 61-col. 5, ln. 15). An insulating film (134) covers the surface of the first conductive film and a second conductive film (136) covers the insulating film (Fig. 4; col. 5, ln. 16-21).

In reference to claim 42, Schoenfeld discloses forming an element active region and an element isolation structure (104) on a semiconductor substrate (102) (Fig. 1; col. 4, ln. 19-23). A gate oxide film (106) and a gate electrode (116) are formed in the active region and an impurity is doped into the substrate in the active region to form a pair of impurity diffusion layers (108/110) in the surface of the substrate on two sides of the gate electrode (Fig. 1; col. 4, ln. 23-31). A first conductive film (128) is electrically connected to one of the impurity diffusion layers (col. 4, ln. 55-58). A mask pattern (130) having first (142) and second (142) openings is formed on the first conductive film and the mask is used to divide the first conductive film below the first opening while simultaneously forming a hole through the first conductive film below the second opening (Fig. 2-3; col. 4, ln. 61-col. 5, ln. 15). A dielectric film (134) covers the surface of the first conductive film and a second conductive film (136) covers the dielectric film (Fig. 4; col. 5, ln. 16-21).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. in view of Wolf et al. (Vol. 1).

In reference to claim 38, Komori discloses a first step of forming element active regions and element isolation structures (4) on a semiconductor substrate (1) (Fig. 2). A second step comprises forming an insulating film (6) on the substrate in the element active region (Fig. 2). A third step comprises forming a first conductive film (7A) on an entire surface including the insulating film and the element isolation structure (col. 8, ln. 7-11). In a fourth step, the first conductive film is patterned such that element isolation regions are exposed (Fig. 3, col. 8, ln. 14-15). Next, a dielectric film (8) is formed so as to cover the first conductive film and a second conductive film (9A) is formed on the dielectric film (Fig. 4; col. 8, ln .21-35). Komori does not disclose the particular steps involved in patterning the first conductive layer. Wolf discloses that the conventional method of patterning a film in semiconductor device fabrication is by photolithography, wherein a mask is formed on the film to be etched, a pattern of openings is formed in the mask by selective light irradiation, and the film is etched in the portions exposed by the mask pattern (pg. 407-408). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a conventional photolithography process to pattern the first conductive film of Komori because, in the absence of the disclosure of any particular process, one of ordinary skill in the art would look to use a conventional process to accomplish the patterning. Using a conventional photolithography process to pattern the first conductive film of Komori would involve forming a mask having at least first and second openings on the first

conductive film and etching the first conductive film in the regions exposed by the openings. As can be seen in Fig. 3, the first conductive film is patterned such that element isolation regions are exposed in the areas from which the first conductive is etched away.

In reference to claim 39, after the second conductive layer is deposited, Komori discloses doping an impurity into the substrate in the element active regions to form a pair of impurity diffusion regions (11n/12n/13p/14n) on each side of the first conductive film (Fig. 6; col. 8, ln. 57-col. 9, ln. 25).

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. in view of Wolf et al. (Vol. 1), as applied to claim 38 above, and further in view of Wolf (Vol. 2).

In reference to claim 40, Komori does not disclose planarizing the first conductive layer by polishing. Wolf (Vol. 2) discloses that when photolithography is used to pattern IC features, it is required that the imaging surface to be etched is very flat in order to obtain the maximum resolution from the photolithography etching process (last paragraph pg. 65, pg. 203). The Examiner takes official notice that chemical mechanical polishing is a well known and conventional method in the art for providing planarization of films. At the time of the invention, it would have been obvious to one of ordinary skill in the art to planarize the first conductive layer of Komori because, as Wolf teaches, it is required that an imaging surface be planar when it is to be subjected to a photolithographic process in order to achieve the maximum resolution from the etching process. Furthermore, it would have been obvious to one of ordinary skill in the art to conduct the planarization using a polishing technique because it is a conventional method of planarization.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. in view of Wolf et al., as applied to claim 38 above, and further in view of Eaton, Jr. et al. (US 4,570,331, previously cited)

In reference to claim 41, Komori discloses forming element isolation regions (4) by performing field oxidation (Fig. 1; col. 7, ln. 64-67). Eaton also discloses a method of forming element isolation regions. However, Eaton teaches that by using field shield isolation structures instead of field oxidation regions, the space between element active regions can be decreased, thereby decreasing the overall size of the semiconductor device (Fig. 3; col. 2, ln. 46-col. 3, ln. 42). Eaton also teaches that this decrease in the space between adjacent element active regions provides "a significant advantage" over the typical field oxidation process (col. 4, ln. 62-68). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the field shield isolation structures of Eaton for the field oxide regions of Schoenfeld because Eaton teaches that field shield isolation structures are superior to field oxidation regions for the purpose of forming element isolation regions because the field shield structures allow the space between adjacent element active regions to be decreased.

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al.

In reference to claim 43, Schoenfeld discloses forming a hole in the insulating interlayer that exposes one of the impurity diffusion layers (Fig. 1). The first conductive film is formed on the insulating interlayer and fills the hole in the interlayer. The first conductive film is etched until the insulating interlayer is exposed in the first and second opening.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. in view of Wolf (Vol. 2).

In reference to claim 44, Schoenfeld does not disclose planarizing the first conductive layer by polishing. Wolf (Vol. 2) discloses that when photolithography is used to pattern IC features, it is required that the imaging surface to be etched is very flat in order to obtain the maximum resolution from the photolithography etching process (last paragraph pg. 65, pg. 203). The Examiner takes official notice that chemical mechanical polishing is a well known and conventional method in the art for providing planarization of films. At the time of the invention, it would have been obvious to one of ordinary skill in the art to planarize the first conductive layer of Schoenfeld because, as Wolf teaches, it is required that an imaging surface be planar when it is to be subjected to a photolithographic process in order to achieve the maximum resolution from the etching process. Furthermore, it would have been obvious to one of ordinary skill in the art to conduct the planarization using a polishing technique because it is a conventional method of planarization.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. in view of Eaton, Jr. et al.

In reference to claim 45, Schoenfeld discloses a method of forming a DRAM semiconductor device in which the element isolation regions (104) are formed by field oxidation (Fig. 1; col. 4, ln. 20-25). Eaton also discloses a method of forming a DRAM structure. However, Eaton teaches that by using field shield isolation structures instead of field oxidation regions, the space between memory cells can be decreased, thereby decreasing the overall size of the semiconductor device (Fig. 3; col. 2, ln. 46-col. 3, ln. 42). Eaton also teaches that this

decrease in the space between adjacent memory cells provides "a significant advantage" over the typical field oxidation process (col. 4, ln. 62-68). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the field shield isolation structures of Eaton for the field oxide regions of Schoenfeld because Eaton teaches that field shield isolation structures are superior to field oxidation regions for use in the DRAM manufacturing process because the field shield structures allow the space between adjacent memory cells to be decreased.

Response to Arguments

Applicant's arguments filed December 27, 2001 have been fully considered but they are not persuasive.

Applicants argue that Schoenfeld fails to anticipate claims 36 and 42 because Schoenfeld does not disclose forming the first opening in the insulating interlayer such that the element isolation structure is exposed. However, claims 36 and 42 do not recite this limitation.

Allowable Subject Matter

Claims 28-31 are allowed.

The primary reasons for the allowance of claims 28-31 is the inclusion therein, in combination as currently claimed, of the limitation of forming a mask pattern on a conductive film that is used to etch the conductive film such that in a first region, the element isolation structure is exposed while, simultaneously, a recess is etched into the first conductive film wherein a portion of the first conductive film remains on the bottom of the recess. This

limitation is found in claim 28 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
March 11, 2002

Michael Trinh
Primary Examiner